CSE 140L Lab 2

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# Academic Integrity

Your work will not be graded unless the signatures of all members of the group are present beneath the honor code.

To uphold academic integrity, students shall:

* Complete and submit academic work that is their own and that is an honest and fair representation of their knowledge and abilities at the time of submission.
* Know and follow the standards of CSE 140L and UCSD.

Please sign (type) your name(s) below the following statement:

I pledge to be fair to my classmates and instructors by completing all of my academic work with integrity. This means that I will respect the standards set by the instructor and institution, be responsible for the consequences of my choices, honestly represent my knowledge and abilities, and be a community member that others can trust to do the right thing even when no one is watching. I will always put learning before grades, and integrity before performance. I pledge to excel with integrity.

(Vincent Ren)

(N/A)

(N/A)

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# Screenshots

## Part 1

### Screenshot of the RTL viewer top level schematic/block diagram in Quartus Or submit your Mentor Precision netlist file if using EDA Playground (3 pts)

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### Please include the output file of part 1 testbench in your submission, and name it “output1.txt” (3 pts)

We will be looking for a text file with that name specifically, so be sure to rename it from “list.txt”. Nothing is required in the writeup for this question.

## Part 2

### Screenshot of the RTL viewer top level schematic/block diagram in Quartus Or submit your Mentor Precision netlist file if using EDA Playground (3 pts)

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### Please include the output file of part 2 testbench in your submission, and name it “output2.txt” (3 pts)

We will be looking for a text file with that name specifically, so be sure to rename it from “list.txt”. Nothing is required in the writeup for this question.

## Part 3

### Screenshot of the RTL viewer top level schematic/block diagram in Quartus Or submit your Mentor Precision netlist file if using EDA Playground (3 pts)

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### Please include the output file of part 3 testbench in your submission, and name it “output3.txt” (3 pts)

We will be looking for a text file with that name specifically, so be sure to rename it from “list.txt”. Nothing is required in the writeup for this question.



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# Free Response

# Please answer the following questions.

## Please write a summary paragraph explaining how you tested your alarm clock in part 1. (4 pts)

It is insufficient to say “I ran the testbench and it worked.” Please tell us what is happening in the testbench and other testing methods that you may have implemented. Word limit: 200 words.

After briefly read the given code, I gave my first try to connect top level logic. Then I ran simulator and checked the wave form. I found that there are some red lines (Z) which means that some signals and input I was not using. Then I read the instruction and the structure diagram, and connected top level again. This time I succeed, and seems like the wave form looks good as well.

Unlike part 2 and 3, part 1 testbench would not have output like “testing set alarm to … .” the only output it has is a transcript recording each change of second/minute/hour. So at that moment I don’t know I have another bug (design flow that I did not notice till submission).

When submitting my code to GradeScope, I was pretty confident. But my part 1 and part 2 alarm set has error. I read instruction again and I found that I did not display alarm time when Alarmset is on. So I added that function to my design, and passed all tests.

## Please write a summary paragraph explaining the day of the week enhancement and how it was implemented. (4 pts)

Word limit: 200 words.

The way I implemented that in my struct\_diag I declare a new submodule recording the day of the week. During compile time, I overwrite that submodule parameter N to 7 representing 7 days in a week. Then the rest would be pretty simple. Just like second/minute/hours, when second/minute/hour advance are all 1, then it’s the time to advance to next day. Since the new submodule has parameter 7, when it’s 6 (Sunday), the next day would be 0 (Monday), because the range of any number mod 7 is 0~6.

## Please write a summary paragraph explaining the date enhancement and how it was implemented. (4 pts)

Word limit: 200 words.

I declare two new modules ct\_mod\_month and ct\_mod\_date. For the second one, it has 3 parameters: X = 31, Y = 30, Z = 28 representing three kinds of months. The increment of date depends on month, so ct\_mod\_date has another input month to help it determines how many days the month has. There is a combinational logic inside it. A logic variable called date\_of\_month would be correctly set depends on month input. If month is 1/3/5/7/8/10/12, date\_of\_month = X = 31, etc. This guarantees that date would function well in particular date. Also, when increment date since we want it to start from 1, we have ct\_next = ct % date\_of\_month + 1;

For ct\_mod\_month, it similar to ct\_mod\_N but with 2 differences. First, parameter is set to 12 since there are 12 months in a year. Second, since we want display starts at 1, so we have ct\_next = ct % N + 1;